CLAIMS

What is claimed is:

1. An electronic substrate for interconnecting electronic components, comprising:

a substrate having one or more conductive inner layers; and

one or more interconnect cavities extending into the substrate to expose one or more of the inner layers.

2. The electronic substrate of claim 1, wherein the substrate further comprises one or more electrically conductive surface layers, wherein one or more of the interconnect cavities extends from one of the surface layers to one or more of the inner layers.

3. The electronic substrate of claim 1, wherein each interconnect cavity comprises a base adjacent to one of the inner layers, the base comprising a layer of electrically conductive material.

4. The electronic substrate of claim 1, wherein each interconnect cavity comprises a base adjacent to one of the inner layers, wherein each interconnect cavity defines a wall, the interconnect cavity further comprising a conductive material forming a liner on the wall and base, the liner interconnected with one or more inner layers.

5. The electronic substrate of claim 1, wherein each interconnect cavity comprises a base adjacent to and electrically interconnected with one of the inner layers, wherein one or more interconnect cavity extending from a surface layer defines a wall, the interconnect cavity further comprising a conductive material forming a liner on the wall and base, the liner interconnected with one or more inner layers and the surface layer.

6. The electronic substrate of claim 1, wherein each interconnect cavity is adapted to receive and interconnect with electrically conductive interconnect material.

7. The electronic substrate of claim 1, wherein the interconnect cavities are positioned to correspond with land pads of a surface mount technology electrical component.

8. The electronic substrate of claim 1, wherein each interconnect cavity comprises a base adjacent to one of the inner layers and an opening at a surface of the substrate, the base having a smaller diameter than the opening.

9. The electronic substrate of claim 1, wherein each interconnect cavitycomprises a base adjacent to one of the inner layers and an opening at a surface of the substrate, the base having a larger diameter than the opening.

10. A method for making a substrate for interconnecting electronic components comprising:

providing a substrate having one or more electrically conductive inner layers; and

forming a cavity extending from a surface of the substrate, the cavity exposing one or more inner layers.

11. The method of claim 10, wherein providing a substrate having one or more electrically conductive inner layers comprises providing a substrate having one or more electrically conductive inner layers and one or more electrically conductive surface layers; and wherein forming a cavity extending from the surface of the substrate, the cavity exposing one or more inner layer comprises forming a cavity extending from one of the surface layers to one or more inner layers.

12. The method of claim 11, further comprises depositing an electrically conductive material to form a liner in the cavity which is interconnected with the corresponding one or more inner layers and the surface layer.

13. The method of claim 12, wherein depositing an electrically conductive material comprises electroplating a layer of conductive material on walls of the cavity.

14. The method of claim 12, wherein depositing an electrically conductive material comprises using a vapor deposition process to form a layer of conductive material on the cavity walls.

15. The method of claim 10, wherein forming a cavity comprises using laser ablation.

16. The method of claim 10, wherein forming a cavity comprises using a resist mask and an etching process.

17. The method of claim 10, wherein forming a cavity comprises forming a cavity with a base having a smaller diameter than an opening at the surface of the substrate.

18. The method of claim 10, wherein forming a cavity comprises forming a cavity with a base having a larger diameter than and opening at the surface of the substrate.

19. An electronic device comprising:
an electronic component having component interconnects; and
an electronic substrate for interconnecting electronic components comprising:
a substrate having one or more conductive inner layers; and

one or more interconnect cavities extending into a surface of the substrate to expose one or more of the inner layers.

20. The electronic device of claim 19, wherein the substrate further comprises one or more electrically conductive surface layers, wherein one or more of the interconnect cavities extends from one of the surface layers to one or more of the inner layers.

21. The electronic device of claim 19, wherein each interconnect cavity comprises a base adjacent to one of the inner layers, the base comprising a layer of electrically conductive material.

22. The electronic device of claim 19, wherein each interconnect cavity comprises a base adjacent to one of the inner layers, wherein each interconnect cavity defines a wall, the interconnect cavity further comprising a conductive material forming a liner on the wall and base, the liner interconnected with one or more inner layers.

23. The electronic device of claim 19, wherein the electronic component is a microelectronic die.